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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/689,824	10/13/2000	Takaaki Sasaki	PNET.011D	7074

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EXAMINER	
LE, DUNG ANH	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/689,824	SASAKI, TAKAAKI	
	Examiner	Art Unit	
	DUNG A LE	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2003* .

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7- 15 and 24-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7- 15 and 24-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

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DETAILED ACTION

Applicants canceled claims 1- 6 and 16- 23, amended claims 7-8, 10, 11, 12, 13, 14, 15, 25, 26 and 27 in Amendment dated 1/6/2004. Claims 7- 15 and 24- 27 are pending in this application.

Based on the new reference, this Office Action is a new ground of the rejection. The previous Office action has been withdrawn.

Set of claims 1-6 (Cancelled).

Set of claims 7-15

Claims 7- 15 are rejected under 35 USC 102 (e) as being anticipated by Miyazaki et al. (6642083).

Miyazaki et al. discloses a method of manufacturing a semiconductor device with a semiconductor element fixed to a semiconductor package, comprising :

preparing said semiconductor package structured by providing a substrate for mounting said semiconductor element 1 thereon to fix said semiconductor element to one side thereof and a connecting pattern provided on the other side of said substrate and by forming a through hole 6 from the one side to the other side of said substrate;

fixing a surface of said semiconductor element to the one side of said substrate of said semiconductor package such that an electrode 7 of said semiconductor element 1 is within said through hole 6;

electrically connecting said connecting pattern 11 and said electrode 7 of said semiconductor element via wires through said through hole 6; and

sealing said through hole and said wires with resin. (figs. 2- 10).

Regarding claim 8, wherein said connecting pattern is provided continuously in a plurality of stages and an end portion of said connecting pattern on the at a side of said through hole is provided on a lower stage on the other side of said substrate (fig. 1).

Regarding claim 9, wherein said through hole is a plurality of through holes (Fig. 10).

Regarding claim 10, wherein the surface of said semiconductor element 1 is fixed on the one side of said substrate 3 of said semiconductor package via a tape-bonding material 8.

Regarding claim 11, wherein the surface of said semiconductor element is fixed on the one side of said substrate of said semiconductor package with adhesive 8 (fig. 6).

Regarding Claim 12, wherein the surface of said semiconductor element 1 is fixed on the one side of said substrate of said semiconductor package via a tape-like bonding material 8.

Regarding claim 13, wherein the surface of said semiconductor element 1 is fixed on the one side of said substrate of said semiconductor package via a tape-like bonding material 8

Regarding claim 14, wherein the surface of said semiconductor element 1 is fixed on the one side of said substrate 3 of said semiconductor package with adhesive 8.

Regarding claim 15, wherein the surface of said semiconductor element is fixed on the one side of said substrate of said semiconductor package with adhesive 8.

Set of claims 16- 23 (Cancelled)

Set of claims 24- 25

Claims 24- 25 are rejected under 35 USC 102 (e) as being anticipated by Miyazaki et al. (6642083).

Miyazaki et al. teach a method of manufacturing a semiconductor device, comprising:

providing a substrate 3 having a first surface and a second surface opposed to the first surface, and further having an elongate opening defined therethrough from the first surface to the second surface;

forming a plurality of connecting patterns on the second surface of said substrate, each of the plurality of connecting patterns having a first end; mounting a surface of a semiconductor chip 1 to the first surface of the substrate 3, wherein a plurality of electrodes 7 are located on the surface of said semiconductor chip 1 and wherein the surface of the semiconductor chip 1 is mounted to the first surface of the substrate such

that the plurality of electrodes are aligned over said elongate opening of said substrate; respectively electrically connecting said plurality of electrodes 7 to corresponding ones of said plurality of patterns by a plurality of wires 11 extending within the elongate opening of said substrate; and covering said plurality of electrodes 7, said plurality of wires 11, and the first ends of said plurality of connecting patterns with a resin. (Figs. 1-10)

Regarding claim 25, wherein said substrate is provided so as to include an upper plate and a lower plate which define a step configuration in the second surface of said substrate, wherein the upper plate is located between said semiconductor chip and said lower plate, and wherein the plurality of connecting patterns are formed so as to extend continuously from said upper plate to said lower plate such that the first end of the plurality of connecting patterns are located on said upper plate (fig. 6- 10)

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Set of claims 26- 27.

Claims 26- 27 are rejected under 35 USC 102 (e) as being anticipated by Miyazaki et al. (6642083).

Miyazaki et al. disclose a method of manufacturing a semiconductor device, comprising: providing a substrate 3 having a first surface and a second surface opposed to the first surface, and further having at least first and second elongate openings defined therethrough from the first surface to the second surface; forming a plurality of connecting patterns on the second surface of said substrate 3, each of the plurality of

connecting patterns having a first end; mounting a surface of a semiconductor chip1 to the first surface of the substrate, wherein a plurality of electrodes 7 are located on the surface of said semiconductor chip and wherein the surface of the semiconductor chip is mounted to the first surface of the substrate such that each of the plurality of electrodes 7 is aligned over one of said first and second elongate openings of said substrate 1; respectively electrically connecting said plurality of electrodes 7 to corresponding ones of said plurality of patterns by a plurality of wires 11 extending within the first and second elongate openings of said substrate; and covering said plurality of electrodes 7, said plurality of wires 11, and the first ends of said plurality of connecting patterns with a resin. (figa. 1- 10)

Regarding claim 27, wherein said substrate is provided so as to include an upper plate and a lower plate which define a step configuration in the second surface of said substrate 3, wherein the upper plate is located between said semiconductor chip 1 and said lower plate, and wherein the plurality of connecting patterns are formed so as to extend continuously from said upper plate to said lower plate such that the first end of the plurality of connecting patterns are located on said upper plate.(figs. 6- 10).

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Friday 8:00am- 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DUNG A. LE
Primary Examiner
Art Unit 2818